A compact, versatile, miniature timing microsystem using two co-integrated wafer-level packaged silicon resonators

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This paper presents a miniature timing microsystem based on a pair of 300µm thick, wafer-level packaged, co-integrated low and high frequency silicon resonators operating at 432kHz and 26.7MHz respectively. Over 700 singulated such parts were flip-chip bonded on a CMOS wafer using thermo-compression on Au stud bumps and the resulting system was calibrated at wafer level and characterized over temperature.

Legacy quartz crystals have recently continuously been challenged by the announcement of new products relying on silicon MEMS resonators for either programmable HF clocks generation or to implement low power real time clocks. The novelty of this work resides in the compact implementation of both functions using a pair of wafer-level packaged co-integrated silicon resonators that are flip-chip bonded on their corresponding CMOS ASIC die at wafer scale to form a mass-producible, miniature, versatile timing microsystem.

The resonators relying on aluminum nitride piezo-actuation are built on 6'' SOI wafers on top of buried cavities and are encapsulated under high vacuum at wafer level using Au-Sn eutectic bonding. After cap wafer back-grinding, tapered TSV are formed from the outer surface before a RDL and contact pads are patterned. The wafer stack is further thinned to 300µm and singulated. Packaged resonator dies are machine-mounted on a CMOS wafer pre-equipped with Au stud bumps using thermo-compression bonding. A micrograph of the resulting microsystem is shown in Figure 1.

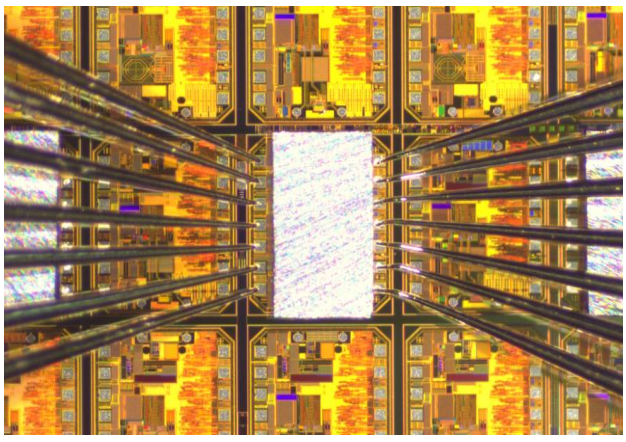

Fig. 1: Micrograph of the timing microsystem taken during wafer level calibration. Size is 1.25x1.6mm.

Automatic wafer level calibration at multiple temperatures using a dedicated probe-card is then performed to determine and compensate electronically for the manufacturing tolerances and temperature behavior of both the dual resonators and circuit via programmable dividers. Corresponding coefficients are stored in an on-chip non-volatile memory. Several temperature cycles are eventually performed while reprogramming different clock frequency outputs to determine the compensation accuracy which reached <±5ppm over -25 to 75°C for both clocks. The LF and HF oscillator consumption is 0.5 and 200µA respectively while the overall system draws 1µA and 5mA in temperature compensated RTC and high frequency clock generation mode via a fractional PLL.