Phase noise and jitter in digital electronics

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We tested a few digital integrated circuits of different technology and families with the ultimate target of understanding low phase noise frequency synthesis. Digital electronics is appealing for its simplicity, reproducibility and cost, in applications where the lower noise of analog circuits is not mandatory. Our work is partially driven by the attempt of reducing the phase noise in two ways. First, by paralleling numerous gates, as in microwave and RF amplifiers[1]. Secondly, to de-alias the output as we did in the Λ divider[2], yet with the largest pipeline made possible by the high toggling frequency of the newest FPGAs (≈1 GHz).

We have identified two classes of phase noise behavior in complex digital devices: 1) the φ-type noise whose power spectral density (PSD) $S\varphi(f)$ is not affected by the carrier frequency ν_0 and 2) the x-type noise that is a fluctuation of the delay and has a PSD $Sx(f)$ independent of ν_0, thus $S\varphi(f) \sim \nu_0^2$. The first case is mostly related to the random voltage (threshold) fluctuation, while the second one is dominated by the signal propagation along the complex path of the clock-distribution subsystem. We have also considered the inherent sampling of digital electronics[2] that introduces aliasing and thus a proportionality factor $1/\nu_0$ to both $Sx(f)$ and $S\varphi(f)$. As a consequence, the two noise types split into four sub-types listed in Table I.

Noise type	Dependence on ν_0	
	$S\varphi(f)$	$Sx(f)$
Pure x-type	ν_0^2	C vs. ν_0
Aliased x-type	ν_0	$1/\nu_0$
Pure φ-type	C vs. ν_0	$1/\nu_0^2$
Aliased φ-type	$1/\nu_0$	$1/\nu_0^3$

Table 1: Basic noise types

With these basic considerations it is possible to characterize logic components by considering phase noise plots as the one reported in Fig. 1 where ν_0 has been changed in a wide range. We measured several logic families. The lowest phase noise is observed in elderly MAX3000 CPLDs based on 300-nm technology. Oppositely, the highest phase noise was found in the highest-density device we tested (28-nm, the FPGA inside a Zynq). This rather general behavior is only partially a surprise because the node size is clearly related to the volume of the active region, where gain and threshold decision take place in analogy to what happens in μW and RF amplifiers[1].

Our work is still in progress, and we will release more at the meeting.

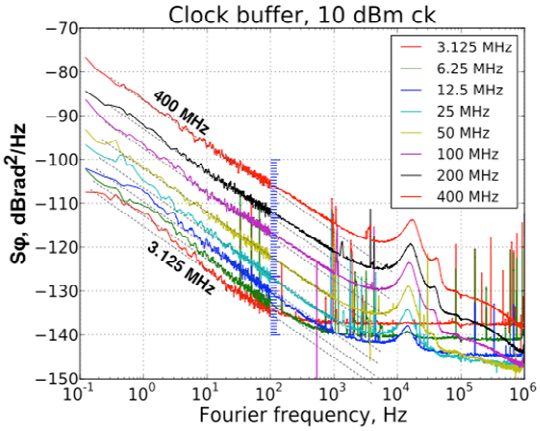

Fig. 2: Phase noise of the Cyclone III FPGA configured as clock buffer.

[1] Boudot, E. Rubiola, Phase noise in RF and microwave amplifiers, IEEE Transact. Ultrason., Ferroelect. Frequency Control, Vol. 59 No. 12, Dec 2012.

[2] C. E. Calosso, E. Rubiola, The sampling theorem in Π and Λ dividers, Proc. IFCS 2013 p. 960-962, Praha, Czech Republic, 21-25 July 2013.